What is claimed is:

1. A Bit Rate Agile (BRA) structure comprising:

a input port for receiving input data;

a splitter having an input coupled to said input port, and serving to split said input data into baseband signal streams;

a baseband signal processing network for receiving said baseband signal streams and providing cross-correlated and filtered Bit Rate Agile (BRA) in phase and quadrature phase baseband signals;

a Quadrature Modulator serving to quadrature modulate said cross-correlated filtered in phase and quadrature phase baseband signals;

an interface transmitter port to provide said quadrature modulated signal to the transmission medium;

an interface receiver port to provide connection of the said cross-correlated filtered quadrature modulated signal to the demodulator; and

a demodulator structure to serve for Bit Rate Agile (BRA) signal demodulation having Bit Rate Agile (BRA) demodulation filters Mis-Matched (MM) to that of the modulator filters.

2. The structure as in Claim 1 wherein said processed in phase and quadrature phase baseband signals have amplitudes such that their vector sum is substantially constant and has reduced resultant quadrature modulated envelope fluctuations.

3. The structure as in claim 1 which further comprises means for selectively reducing the cross correlating factor down to zero.

4. A cross-correlated signal processor for Bit Rate Agile (BRA) and Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) means comprising:

(a) means for providing in-phase and quadrature phase signals;

(b) means for cross-correlating a fraction of a symbol or one or more than one symbol of the in-phase (I) signal with a fraction of a symbol or one or more than one symbol of the quadrature-phase (Q) signal;

(c) means for generating filtered cross-correlated I and Q signals;

(d) means for implementing the cross-correlated signals by analog active or passive circuits, by digital circuits or combination thereof;

(e) means for providing a control circuit to select from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels;

(f) means for Quadrature modulating the I and Q signals;

(g) means for Linear and/or Nonlinear amplification to provide to the antenna;

(h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator;

(i) a BRA and MFS quadrature demodulator; and

(j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the said demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

5. Cross-correlated signal processor means for Bit Rate Agile (BRA) and Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) means comprising:

(a) processing means for one or more input signals and providing in-phase (I) and quadrature phase (Q) signals;

(b) means for cross-correlating the in-phase and quadrature shifted signals;

(c) means for generating in-phase and quadrature shifted output signals having amplitudes such that the vector sum of the output signals is approximately the same at virtually all phase angles of each bit period for one set of cross-correlation and filter parameters and the vector sum is not constant for an other set of chosen filter parameters;

(d) means for quadrature modulating the in-phase and quadrature output signals, to provide a cross-correlated modulated output signal;

(e) means for providing a control circuit to select from a set of predetermined cross-correlated signal elements filters and selectable waveforms in the I and/or Q channels;

(f) means for Quadrature modulating the I and Q signals;

(g) means for Linear and/or Nonlinear amplification to provide to the antenna

(h) a receiver port for connection of the received cross-correlated signal to the BRA and MFS demodulator;

(i) a BRA and MFS quadrature demodulator; and

(j) a Mis-Matched (MM) BRA and MFS demodulator filter set in which the demodulator filter set is MM to that of the BRA and MFS filter set of the modulator.

6. A cross-correlated signal processor comprising:

(a) means for cross-correlating a fraction, or one or more than one symbol synchronous and/or asynchronous time constrained signal (TCS) response and cascaded long response (LR) filtered signal symbols of one or more input signals with signal symbols of a quadrature phase shifted signal of the in-phase signal, and providing in-phase (I) and quadrature phase (Q) shifted signals for Bit Rate Agile (BRA), cascaded mis-matched (ACM) Modulation-Demodulation (Modem) Format Selectable (MFS) and Code Selectable (CS) processing, according to the following schedule:

(i) when the in-phase channel signal is zero, the quadrature shifted signal is close to the maximum amplitude normalized to one (1);

(ii) when the in-phase channel signal is non-zero, the maximum magnitude of the quadrature shifted signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$;

(iii) when the quadrature channel signal is zero, the in-phase signal close to the maximum amplitude;

(iv) when the quadrature channel signal is non-zero, the in-phase signal is reduced from 1 (normalized) to A, where $0 \leq A \leq 1$;

(b) means for quadrature modulating the in-phase and quadrature output signals to provide a cross-correlated modulated output signal;

(c) controlling means and signal selection means for BRA rate, MFS and CS processor selection and selection for Linear and/or Non-Linearly Amplified(NLA) baseband and/or of Quadrature modulated signals;

(d) coupling port means to the transmission medium;

(e) a receiver port for connection of the received cross-correlated signal to the BRA, MFS and CS demodulator;

(f) a BRA, MFS and CS quadrature demodulator; and

(g) a Mis-Matched (MM) demodulator filter set for BRA, MFS and CS in which the said demodulator filter set is MM to that of the BRA, MFS and BRA filter set of the modulator.

7. A structure comprising:

an interface receiver port to provide connection of received Bit Rate Agile (BRA) cross-correlated filtered quadrature modulated signal to the demodulator; and

a demodulator structure to serve for signal demodulation of said signal.

8. An adaptive equalizer structure comprising:

an interface receiver port to provide connection of received modulated signal to the pre-demodulation adaptive equalizer;

a pre-demodulation adaptive equalizer structure comprising splitter, multiplier and delay structure for generating a control signal and received modulated signal time delayed product in one branch of the splitter and coupling the signal time delayed product in one branch of the splitter and the said received modulating signal in the other branch of the splitter to a signal combiner;

a signal combiner structure for combining the said delayed control signal and received modulated signal product;

a demodulator structure for demodulating the combined delayed control signal and received modulated signal product; and

a control signal processor for generation of and connection of said control signal to the said product multiplier circuit.

9. An adaptive equalizer and switchable delay structure comprising:

an interface receiver port to provide connection of received modulated signal to a plurality of splitters, amplifiers, delay elements and signal combiners for signal selection of said received modulated signal;

a demodulator structure for demodulating the selected received modulated signal; and

a control signal processor for generation of said control signal.

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